Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A programmable logic device, comprising a plurality of logic elements and a routing structure, wherein the routing structure comprises a plurality of routing lines, and wherein each routing line comprises:

a plurality of first OR gates, each first OR gate having at least a first input connected to a respective one of said logic elements in a first group of said logic elements, and each first OR gate except a final first OR gate in said line having an output connected to a second input of a respective succeeding one of said first OR gates, such that a signal from one of said logic elements in the first group of logic elements appears on an output of the final first OR gate in said line; and

a return line, comprising a plurality of drivers connected in series, each of said drivers having a connection to a respective one of a plurality of said logic elements in a second group of logic elements, such that the signal appearing on said output of the final first OR gate in said line may be passed to said plurality of logic elements in the second group of logic elements.

2. (original) A programmable logic device as claimed in claim 1, wherein the first group of logic elements and the second group of logic elements are mutually exclusive.

3. (original) A programmable logic device as claimed in claim 1, wherein the first group of logic elements and the second group of logic elements contain at least one logic element in common.

4. (original) A programmable logic device as claimed in claim 1, wherein the logic elements in said programmable logic device are arranged in an array, the array comprising rows and columns of logic elements.

5. (original) A programmable logic device as claimed in claim 4, wherein the first group of logic elements are located within a first row of said array.

6. (original) A programmable logic device as claimed in claim 5, wherein the second group of logic elements are located within said first row of said array.

7. (original) A programmable logic device as claimed in claim 5, wherein the second group of logic elements are located within a second row of said array different from said first row.

8. (original) A programmable logic device as claimed in claim 5, wherein the first group of logic elements are spaced apart at regular intervals within said first row of said array.

9. (original) A programmable logic device as claimed in claim 7, wherein the second group of logic elements are spaced apart at regular intervals within said second row of said array.

10. (original) A programmable logic device as claimed in claim 4, wherein the first group of logic elements are located within a first column of said array.

11. (original) A programmable logic device as claimed in claim 10, wherein the second group of logic elements are located within said first column of said array.

12. (original) A programmable logic device as claimed in claim 10, wherein the second group of logic elements are located within a second column of said array different from said first column.

13. (original) A programmable logic device as claimed in claim 10, wherein the first group of logic elements are spaced apart at regular intervals within said first column of said array.

14. (original) A programmable logic device as claimed in claim 12, wherein the second group of logic elements are spaced apart at regular intervals within said second column of said array.

15. (previously presented) A programmable logic device, comprising:

a plurality of logic elements arranged in an array, the array comprising rows and columns of logic elements, the rows of said array being located at respective vertical positions in said array, and the columns of said array being located at respective horizontal positions in said array; and

a routing structure, wherein the routing structure comprises a first plurality of routing lines, running parallel to said rows of logic elements at a first vertical position in said array; a second plurality of routing lines, running parallel to said rows of logic elements at a second vertical position in said array; a third plurality of routing lines, running parallel to said columns of logic elements at a first horizontal position in said array; and a fourth plurality of routing lines, running parallel to said columns of logic elements at a second horizontal position in said array,

wherein each routing line comprises:

a plurality of first OR gates, each first OR gate having at least a first input connected to a respective one of said logic elements in a respective first group of said logic elements, and each first OR gate except a final first OR gate in said line having an output connected to a second input of a respective succeeding one of said first OR gates, such that a signal from one of said logic elements in the first group of logic elements appears on an output of the final first OR gate in said line; and

a return line, comprising a plurality of drivers connected in series, each of said drivers having a connection to a plurality of said logic elements in a respective second group of logic elements, such that the signal appearing on said output of the final first OR gate in said line may be passed to said plurality of logic elements in the second group of logic elements.

16. (original) A programmable logic device as claimed in claim 15, wherein routing lines of said first plurality of routing lines and of said second plurality of routing lines are connected to respective logic elements spaced apart along said rows of logic elements; and

routing lines of said third plurality of routing lines and of said fourth plurality of routing lines are connected to respective logic elements spaced apart along said columns of logic elements.

17. (canceled).

18. (previously presented) In a programmable logic device, comprising a plurality of logic elements and a routing structure, wherein the routing structure comprises a plurality of distributed OR gates, each distributed OR gate comprising logic circuitry having a plurality of inputs from a first plurality of logic elements distributed amongst said logic elements and forming a logic OR function from said inputs, and an output of each distributed OR gate being connected to a second plurality of logic elements distributed amongst said logic elements, a method of forming a bus structure, the method comprising:

allocating functionality to said first plurality of logic elements, and to said second plurality of logic elements in a first distributed OR gate; and

controlling said first plurality of logic elements such that they each output a logical zero except when involved in a data transaction,

such that outputs from said first plurality of logic elements are multiplexed together, and made available to said second plurality of logic elements via a return line coupled to an end OR gate of the plurality of distributed OR gates.

19. (original) A method of forming a bus structure, as claimed in claim 18, further comprising:

allocating additional functionality to said first plurality of logic elements, and to said second plurality of logic elements, such that said second plurality of logic elements are connected to the inputs of a second distributed OR gate and the output of the second distributed OR gate is connected to the first plurality of logic elements; and

controlling said second plurality of logic elements such that they each output a logical zero except when involved in a data transaction,

such that outputs from said second plurality of logic elements are multiplexed together, and made available to said first plurality of logic elements.

20. (original) A method of forming a bus structure, as claimed in claim 19, comprising allocating functionality to said first plurality of logic elements such that they form parts of respective bus master devices, and allocating functionality to said second plurality of logic elements such that they form parts of respective slave devices in said bus structure